Engineer-to-Engineer Note   EE-68

Analog Devices JTAG Emulation Technical Reference

Contributed by David M. Doyle   *Rev 10 – April 15, 2008*

Introduction

This document provides technical information to properly design a JTAG emulator interface for Analog Devices, Inc. (ADI) processor targets, which are all referred to as *digital signal processors (DSPs)* in this document. For an introduction to the IEEE 1149.1 (JTAG) standard, see Appendix E: Introduction to IEEE Std. 1149.1 (JTAG) Boundary Scan.

ADI designs, manufactures, and sells several different types of JTAG emulators for use with ADI DSP targets supporting an embedded JTAG emulator port. This document has been revised to only support the current line of ADI emulators. This product line includes the HPPCI, HPUSB, and USB emulators.

Previous versions of this document supported ADI JTAG emulator legacy products such as *Mountain-ICE*, *Summit-ICE*, *Trek-ICE*, *Apex-ICE*, and *EZ-ICE*. For information about JTAG emulators not supported by this document, contact ADI's DSP development tools technical support (processor.tools.support@analog.com) for an older version of this document that has legacy JTAG emulator information.

> Do not use older versions of EE-68 for new target designs. Periodically, check ADI's Web site for the latest version of this document. Targets designed using an older version of EE-68 should only be updated if there are problems performing JTAG emulation.
>
> http://www.analog.com/ee-notes/

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JTAG Emulator Interface Design

All ADI JTAG emulators interface with the DSP using a 14-pin JTAG emulator header. The header provides a connection interface for the JTAG emulator pod. The header can also be used to connect an optional local (embedded on the user target) boundary scan controller to the DSP when the JTAG emulator is not attached.

All ADI JTAG emulators use a superset of the IEEE 1149.1 standard to send and receive data from the DSP JTAG emulation port. JTAG emulators use an additional signal called EMU~ as a JTAG emulation status flag from the DSP. This signal is a vendor-specific signal, which is not part of the IEEE 1149.1 specification.

The following pages define in detail the design requirements for supporting ADI JTAG emulators. This information includes functional, electrical, and mechanical requirements for interfacing a target design with a JTAG emulator.

JTAG Emulator Target Header

Referring to Figure 1 and Table 1, the JTAG emulator header has 14 pins. You must supply this header on your target to communicate with the JTAG emulator. The JTAG emulator target header interface is a standard dual-row 0.025" male square-post header, employing 0.1" x 0.1" spacing, with a minimum post length of 0.235". Pin 3 of the JTAG emulator cable header is keyed to prevent accidental insertion of the pod with the target backwards. You should clip pin 3 on your target board header to allow insertion of the JTAG emulator cable female header.

> ⓘ The JTAG emulator 14-pin female header position 3 connects to a wire in the JTAG cable, which returns to ground at the emulator.

Figure 1. JTAG emulator target header interface

Local Boundary Scan Controller

Referring to Figure 1, the set of signals on the odd-numbered side of the connector can be used by targets which have an optional local boundary scan controller. These signals include the boundary-scan controller JTAG signals BTMS/VDDIO, BTCK, BTDI, and BTRST~. Each of these signals is described in Table 1.

> ⓘ If you are unfamiliar with local boundary scan and how it may apply to your design, see Appendix E: Introduction to IEEE Std. 1149.1 (JTAG) Boundary Scan.

Special Case Pin 5 BTMS

Pin 5 BTMS/VDDIO is a dual-purpose pin on the HPPCI JTAG emulator. First, it allows you to route an optional local boundary scan controller TMS signal to the target DSP TMS signal when the JTAG ICE is not attached to the JTAG header and a jumper is installed between pins 5 and 6 of the JTAG header. Second, this pin is used by the JTAG ICE to auto detect the targets DSP I/O voltage (VDDIO) up to 5 V. The JTAG ICE uses the sensed voltage to establish input and output voltage levels for the DSP JTAG signals. Pull this pin up to VDDIO using a 4.7-KΩ resistor. Do not connect it directly to the VDDIO plane.

> ⓘ Only the HPPCI JTAG emulator supports automatic voltage sensing with pin 5. The USB and HPUSB JTAG emulator's pin 5 only supports the BTMS functionality.

Pin	Signal	Description	Emulator	Target
1	GND	Digital ground	Passive	Passive
2	EMU~	JTAG emulation flag	Input *{active low}*	Output *{open drain} {active low}*
3	KEY	Header alignment position -- pin must be clipped on target header	GROUND	No Connect
4	GND	Digital ground	Passive	Passive
5	VDDIO or BTMS	Automatic voltage sense (VDDIO) or Target local boundary scan controller JTAG TAP test mode select	Input	Passive or Output
6	TMS	JTAG TAP test mode select	Output	Input
7	BTCK	Target local boundary scan controller JTAG TAP test clock	No Connect	Output
8	TCK	JTAG TAP test clock	Output	Input
9	BTRST~	Target local boundary scan controller JTAG TAP test reset	No Connect	Output *{active low}*
10	TRST~	JTAG TAP test reset	Output	Input *{active low}*
11	BTDI	Target local boundary scan controller JTAG TAP test data in	No Connect	Output
12	TDI	JTAG TAP test data in	Output	Input
13	GND	Digital ground	Passive	Passive
14	TDO	JTAG TAP test data out	Input	Output

Table 1. JTAG emulator header signal descriptions

BTMS Pin VDDIO Auto-Detect Function

The HPPCI JTAG emulator can automatically sense a DSP IO voltage (VDDIO) up to 5 V. The HPPCI JTAG emulator uses the VDDIO voltage it senses from the BTMS/VDDIO pin to adjust the JTAG emulator interface input signal thresholds and output signal drive levels to those shown in Table 2. You must pull pin 5 (BTMS/VDDIO) up to the DSP I/O voltage (VDDIO) with a 4.7-KΩ resistor when using the HPPCI JTAG emulator.

When using the HPUSB and USB JTAG emulators which do not support VDDIO auto-sensing, you can connect pin 5 directly to the target local boundary scan controller BTMS signal without any pull-up resistor required.

VDDIO is the target DSP I/O voltage supply, not the DSP core voltage supply. Ensure that you connect VDDIO to the correct voltage plane when using the HPPCI VDDIO auto-sense function.

BTMS Pin Boundary Scan Function

Pin 5 can be used to route an optional local boundary scan controller TMS signal to the target DSP TMS signal when the JTAG ICE is not attached to the JTAG header and a jumper is

installed between pins 5 and 6 of the JTAG header.

You may connect an HPUSB or USB JTAG emulator to a target designed for the HPPCI JTAG emulator with the VDDIO auto-sensing logic. The HPUSB or USB JTAG emulator does not connect pin 5 back at the emulator, so the target or emulator will not be harmed. The voltage thresholds for your target when using the HPUSB or USB JTAG emulators are set manually by the user in the VisualDSP++® Session Wizard.

(i) When using the HPPCI JTAG emulator, you need to control the BTMS signal at pin 5 so that it is not being driven by the local boundary scan controller when the JTAG ICE is attached to the header. Failure to isolate the BTMS signal when the JTAG ICE is connected could result in unpredictable behavior by the JTAG ICE due to possible incorrect voltage sensing on pin 5. As shown in Figure 8 and Figure 9, you can isolate the BTMS signal using a jumper or a buffer. When using a buffer, its output must be disabled when the JTAG ICE is connected.

JTAG Emulator Pod Mechanical Requirements

This section explains the mechanical specifications for the JTAG emulator pod.

JTAG Emulator Header Clearance Requirements

Provide a clearance of at least 0.30" and 0.10" around the length and width of the header. Refer to Figure 2 for information about the pod connector keep out area.

(i) Allow for height clearance above the header for attaching and detaching the JTAG emulator cable from your target.
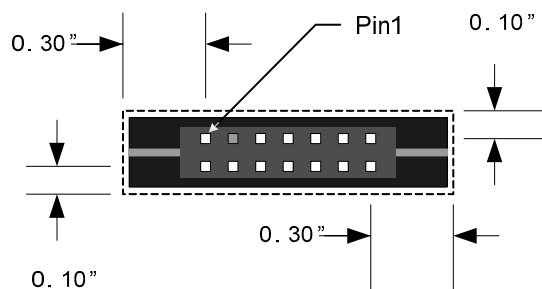

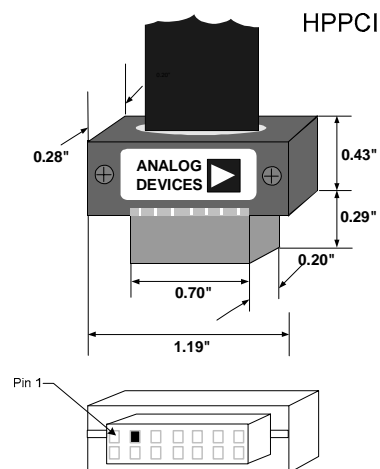Figure 2. JTAG emulator header keep-out area

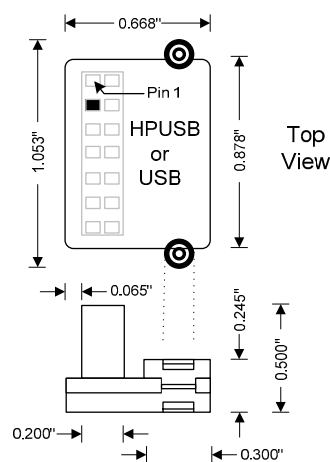Figure 3. HPPCI JTAG emulator pod dimensions

Figure 4. JTAG HPUSB JTAG emulator pod dimensions

Refer to Figure 3 for height clearance restriction information regarding the HPPCI JTAG emulator cable. Refer to Figure 4 for any height clearance restriction information for the HPUSB and USB JTAG emulators.

Target JTAG Emulator Pod Interface Design Requirements

This section defines how to design the JTAG emulator pod interface for different target platforms. The targets include single or multiple DSP targets with or without local boundary scan logic.

Refer to the following Appendix sections of this document regarding the JTAG emulator pod interface design requirements for the type of target you are designing.

- Appendix A: Target JTAG Interface Design - Single DSP Target without Boundary Scan

- Appendix B: Target JTAG Interface Design - Multiple DSP Target without Boundary Scan

- Appendix C: Target JTAG Interface Design - Single DSP Target with Boundary Scan

- Appendix D: Target JTAG Interface Design - Multiple DSP Target with Boundary Scan

JTAG Emulator Interface PCB Layout

Treat all JTAG emulator signals (TCK, TMS, TDI, TDO, EMU~, and TRST~) as critical route signals. Pay special attention when routing these signals on your target. Specify a controlled impedance requirement between 50 Ω and 75 Ω. Minimize cross-talk and inductance on these signal lines by using a solid ground plane and routing the JTAG emulator signals away from high-frequency nets, especially clock lines. Keep these routes as short as possible, and equal in length when possible.

These lines must be clean. You may need to provide series terminations for very long TDO and EMU~ routes. See appendixes A through D for information regarding series terminations.

JTAG Emulator Power Sequence

Your JTAG emulator should be powered on, and connected to a host PC, prior to attaching it to a target JTAG emulator header. All ADI high-performance JTAG emulator products can be attached or removed from a powered "hot" target without any power restrictions.

Avoid emulation errors by ensuring that the emulation software is not started or executing when power is not applied to the target, or when attaching the JTAG emulator to a target with or without power.

You must install a 4.7-KΩ pull-down resistor on the TRST~ net going to the DSP per appendixes A through D, except for targets that use boundary scan logic AND do not control the TRST/~ signal.

For targets that use boundary scan logic AND do not control the TRST~ signal, do not pull down the TRST~ signal. Use of this resistor could prevent the boundary scan logic from moving the tap. A jumper should be installed for the TRST~, signal across the JTAG emulator header TRST~ and BTRST~ pins before applying power to the target. Install this jumper whenever the JTAG emulator is not attached to the JTAG emulator header after power has been applied to the target. This jumper prevents the JTAG TAP in the DSP from getting "lost" in an un-recoverable state.

JTAG Emulator Pod Electrical Requirements

This section explains the electrical specifications for the JTAG emulator pod.

HPPCI JTAG Emulator Automatic Voltage Sense Pod Logic

The HPPCI JTAG emulator pod uses pin 5 (BTMS/VDDIO) of the JTAG emulator header to automatically sense the target I/O voltage. The voltage sensing logic controls which voltage threshold values the JTAG emulator uses for JTAG signals received from the target. The voltage sensing logic also sets the drive levels for JTAG signals sent to the target.

Your target DSP IO voltage (VDDIO) may or may not be the same voltage used by the DSP core. Ensure that you are using the correct DSP supply voltage for VDDIO when configuring your target for the HPPCI JTAG emulator automatic voltage sense. You must pull the signal up to the correct voltage plane with a 4.7-KΩ resistor. *Do not* connect the BTMS/VDDIO pin directly to the VDDIO voltage plane. See Appendixes A through D for more information regarding the BTMS/VDDIO pin.

JTAG Emulator Pod I/O Characteristics

The JTAG emulator pod is tolerant up to 5V DC. It will work with all Analog Devices JTAG family DSPs with JTAG I/O voltages of 5 V, 3.3 V, 2.5 V, and 1.8 V. The pod will drive 5-V targets with 3.3-V logic levels, which are well within the 5-V logic threshold requirements. Table 2 includes all the I/O characteristics for the JTAG emulator pod.

Pin	JTAG Emulator Signal	VDDIO (VDC)	Cin (pF)	Cout (pF)	VIH (VDC)	VIL (VDC)	VOH (VDC)	VOL (VDC)	IOL (mA)	IOH (mA)
2	EMU~	5 / 3.3	6		2.0	0.8	-	-	-	-
6	TMS	5 / 3.3		6.5	-	-	2.3	0.7	12	12
8	TCK	5 / 3.3		6.5	-	-	2.3	0.7	12	12
10	TRST~	5 / 3.3		6.5	-	-	2.3	0.7	12	12
12	TDI	5 / 3.3		6.5	-	-	2.3	0.7	12	12
14	TDO	5 / 3.3	6		2.0	0.8	-	-	-	-
2	EMU~	2.5	6		1.7	0.7	-	-	-	-
6	TMS	2.5		6.5	-	-	1.8	0.6	8	8
8	TCK	2.5		6.5	-	-	1.8	0.6	8	8
10	TRST~	2.5		6.5	-	-	1.8	0.6	8	8
12	TDI	2.5		6.5	-	-	1.8	0.6	8	8
14	TDO	2.5	6		1.7	0.7	-	-	-	-
2	EMU~	1.8	6		1.2	0.6	-	-	-	-
6	TMS	1.8		6.5	-	-	1.3	0.5	4	4
8	TCK	1.8		6.5	-	-	1.3	0.5	4	4
10	TRST~	1.8		6.5	-	-	1.3	0.5	4	4
12	TDI	1.8		6.5	-	-	1.3	0.5	4	4
14	TDO	1.8	6		1.2	0.6	-	-	-	-

Table 2. JTAG emulator pod I/O characteristics

JTAG Emulator Pod Timing

This section details important timing information regarding JTAG signals at the target JTAG emulator header. Figure 5 diagrams switching and timing relationships for JTAG signals at the target JTAG emulator header.

Table 3 defines switching parameters for the JTAG emulator output signals (TCK, TMS, TDI,

and TRST~), and setup and hold requirements for JTAG emulator input signals (TDO, and EMU~). Table 3 also defines the frequency of operation range for high performance JTAG emulator products. The table parameter reference numbers maps to the timing diagram reference numbers shown in Figure 5.
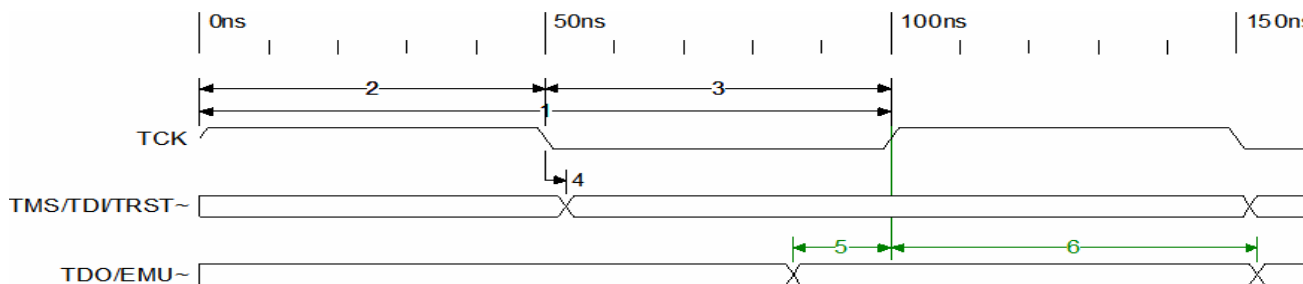

Figure 5. JTAG emulator pod timing waveform

Use this information to determine your target's maximum routing lengths, net loading, and load capacitance which can be tolerated for JTAG emulation signal routes.

The maximum frequency numbers shown in Table 3 are only guaranteed when your target meets the setup and hold requirements defined in Table 3. When calculating your setup and hold margins, be sure to include the TDO and EMU~ delay parameters from the target DSP data sheet. If your target does not meet the setup and hold requirements specified in Table 3, you will have to operate the JTAG emulator at a lower frequency for reliable performance.

(i) If you cannot operate the JTAG emulator using the lowest available frequency, check your target for incorrect wiring, or redesign your target to reduce delays. Try to reduce trace lengths, reduce electrical loads, and use faster buffers.

The setup and hold time requirements are based on the worst-case maximum delay of the JTAG emulator hardware. Typically, the setup and hold time requirements will be considerably smaller

than the values in the table. If you have a complex JTAG emulation path with long propagation delays, perform a timing analysis on your target's JTAG paths. Use this analysis to determine whether your target JTAG emulation paths have sufficient timing margin to operate at the desired JTAG TCK frequency.

When performing a timing analysis, the timing margin must be a positive number. As a general rule, the desired margin should be at least 10% of a full TCK clock period. However, be aware when you are doing your analysis, the delay numbers given are based on worst-case delay. Typically, logic will tend to run somewhere in the middle between minimum and maximum delay, although this cannot be guaranteed. If your margin is negative, but very close (< 1 ns), you may want to try using typical numbers in your analysis to see whether you still have a negative margin.

If you still calculate a negative margin using typical values, try selecting a slower TCK frequency if available, or make changes to your target to reduce the JTAG emulator path delays.

#	Parameter	Product	Frequency	Description	Min. Freq. (ns)	Max. Freq. (ns)
1	t_cTCK	HPPCI	10↔50 MHz	TCK period	*19.9*	*100.1*
1	t_cTCK	HPUSB	5↔50 MHz	TCK period	*19.9*	*200.1*
1	t_cTCK	USB	10 MHz	TCK period	*99.1*	*100.1*
2	t_wTCKH	HPPCI	10↔50 MHz	TCK high pulse width	*9.95*	*50.05*
2	t_wTCKH	HPUSB	5↔50 MHz	TCK high pulse width	*9.95*	*100.05*
2	t_wTCKH	USB	10 MHz	TCK high pulse width	*49.95*	*50.05*
3	t_wTCKL	HPPCI	10↔50 MHz	TCK low pulse width	*9.95*	*50.05*
3	t_wTCKL	HPUSB	5↔50 MHz	TCK low pulse width	*9.95*	*100.05*
3	t_wTCKL	USB	10 MHz	TCK low pulse width	*49.95*	*50.05*
4	tdTMS	HPPCI	10↔50 MHz	Delay TMS/TDI/TRST~ from TCK ↓		3
4	tdTMS	HPUSB	5↔50 MHz	Delay TMS/TDI/TRST~ from TCK ↓		3
4	tdTMS	USB	10 MHz	Delay TMS/TDI/TRST~ from TCK ↓		3
5	tsuTDO	HPPCI	10 MHz	Setup time TDO/EMU~ to TCK ↑	14.1	
5	tsuTDO	HPPCI	25 MHz	Setup time TDO/EMU~ to TCK ↑	1	
5	tsuTDO	HPPCI	33 MHz	Setup time TDO/EMU~ to TCK ↑	8.4	
5	tsuTDO	HPPCI	50 MHz	Setup time TDO/EMU~ to TCK ↑	9.9	
5	tsuTDO	HPUSB	5-50 MHz	Setup time TDO/EMU~ to TCK ↑	2	
5	tsuTDO	USB	10 MHz	Setup time TDO/EMU~ to TCK ↑	2	
6	thTDO	HPPCI	10-50 MHz	Hold time TDO/EMU~ from TCK ↑	0	
6	thTDO	HPUSB	5-50 MHz	Hold time TDO/EMU~ from TCK ↑	0	
6	thTDO	USB	10 MHz	Hold time TDO/EMU~ from TCK ↑	0	

Table 3. JTAG emulator pod timing information

Conclusion

The recommendations in this document should make designing the JTAG emulation interface for your target straight forward. Having a well-designed JTAG emulator interface on your target will allow you to rapidly begin development and testing your application, instead of spending valuable time debugging the JTAG emulation port. Check the ADI DSP Tools Web site periodically for updates to this document.

Appendix A: Target JTAG Interface Design - Single DSP Target without Boundary Scan

This section describes how to design the JTAG emulator pod interface for single DSP targets *without* a local boundary scan controller.

As shown in Figure 6, single DSP targets *without* a local boundary scan controller, or do not include the DSP in a local boundary scan controller chain, should tie all boundary scan pins (except for pin 5) to ground when using the HPPCI JTAG emulator. Pin 5, the BTMS/VDDIO signal, is required by the HPPCI JTAG emulator pod to automatically sense the DSP I/O voltage (VDDIO).

Single DSP targets with routing distances between the JTAG emulator header and the DSP of less than six (6) inches do not require buffering.

ⓘ Buffer your target if the worst-case route distance between the JTAG emulator header and the DSP is greater than six (6) inches, regardless of the number of DSPs in the scan chain path.

Figure 6 shows the connections between the JTAG emulator header and the DSP for a single DSP target *without* a local boundary scan controller.

ⓘ Figure 6 shows series terminating resistors for the TDO and EMU~ signals going to the JTAG emulator. These resistors are optional. Use terminators if the TDO or EMU~ routes are longer than 6 inches between the DSP and the JTAG emulator header.

The terminator resistor value is generally equal to the impedance of the printed circuit board (Z_{PCB}) minus the output impedance of the TDO or EMU~ signal I/O driver (Z_{Driver}). Initially, set these resistors to zero ohms. Change the value of the termination resistance $Z_{Terminator,}$ to Z_{PCB} minus Z_{Driver} if signal integrity problems are observed when using the JTAG emulator. Tuning the termination resistor value to something slightly less than or greater than $Z_{Terminator}$ may be required, depending on the condition of the signals. Place the termination resistors as close to the DSP as possible.

ⓘ Previous versions of this document called for pull-up resistors on TMS, TCK, and TDI. The strong drive strength of the CMOS buffers used in the emulator makes this unnecessary.
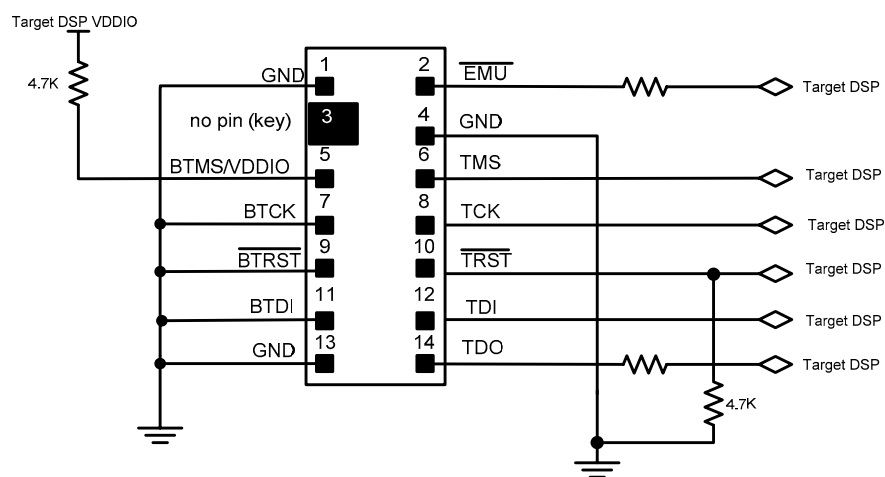

Figure 6. Single DSP target without a local boundary scan controller

Appendix B: Target JTAG Interface Design - Multiple DSP Target without Boundary Scan

This section describes how to design the JTAG emulator pod interface for multiple DSP targets *without* a local boundary scan controller.

As shown in Figure 7, targets with multiple DSPs in the chain and *without* a local boundary should tie all boundary scan pins (except pin 5) to ground when using the HPPCI JTAG emulator. Pin 5, the BTMS/VDDIO signal, is required by the HPPCI JTAG emulator pod to automatically sense the DSP I/O voltage (VDDIO).

As shown in Figure 7, targets with more than one DSP in the scan path, which *do not* use a local boundary scan controller, require buffering. Figure 7 shows the connections between the JTAG emulator header and buffers for a multiple DSP target *without* a local boundary scan controller.

For 5-V targets, buffer the TCK signal with a low-skew, high fan-out, minimal input-to-output delay, dual 1-to-5 clock driver type IDT49FCT805 (or equivalent), and buffer the TMS, TDI, TRST~, TDO, and EMU~ signals with a type 74AC11244 buffer (or equivalent).

For 3.3-V low-voltage targets, buffer the TCK signal with a low-skew, high fan-out, minimal input-to-output delay, dual 1-to-5 clock driver type IDT49FCT3805E (or equivalent), and buffer the TMS, TDI, TRST~, TDO, and EMU~ signals with a type 74AVC16244 buffer (or equivalent).

For 2.5-V / 1.8-V very low voltage targets, buffer the TCK signal with a low-skew, high fan-out, minimal input-to-output delay, single 1-to-5 clock driver type IDT5T9050 (or equivalent), and buffer the TMS, TDI, TRST~, TDO, and EMU~ signals with a type 74AVC16244 buffer (or equivalent).

(i) Figure 7 shows series terminating resistors for the TDO and EMU~ signals going to the JTAG emulator. These resistors are optional. Use terminators if the TDO or EMU~ routes between the buffers and the JTAG emulator header are longer than 6 inches.

The terminator resistor value is generally equal to the impedance of the printed circuit board (Z_{PCB}) minus the output impedance of the TDO or EMU~ signal I/O driver (Z_{Driver}). Initially, set these resistors to zero ohms. Change the value of the termination resistance $Z_{Terminator,}$ to Z_{PCB} minus Z_{Driver} if signal integrity problems are observed when using the JTAG emulator. Tuning the termination resistor value to something slightly less than or greater than $Z_{Terminator}$ may be required, depending on the condition of the signals. Place the termination resistors as close to the DSP as possible.

(i) To minimize signal skew, ensure that buffers for the TMS, TDI, TRST~, TDO, and EMU~ signals come from a single package. For TCK signals, use a driver with a high fan-out. The drivers should come from a single dedicated package that *is not* used by other TMS, TDI, TRST~, TDO, or EMU~ signals.

Route all traces between the JTAG emulator header and the DSP as a group, using equal lengths when possible. Provide good crosstalk isolation from other signal nets especially clocks.

Limit the number of loads (DSPs) for the TMS, TRST~, and EMU~ buffered signals to eight (8). Limit the number of loads for the TCK buffered signals to one (1). Additional loads (DSPs) should use another buffer to support up to eight (8) more devices.

(i) Previous versions of this document called for pull-up resistors on TMS, TCK, and TDI. The strong drive strength of the CMOS buffers used in the emulator makes this unnecessary.

Using more than sixteen (16) physical devices in one scan chain is not recommended. The best approach for large numbers (>16) of physical devices is to break the chain into smaller independent chains, each with its own JTAG header and buffers. If this is not possible, try adding jumpers to reduce the number of devices in one chain at a time for debug purposes. Pay special attention to PCB routing to minimize transmission line effects.
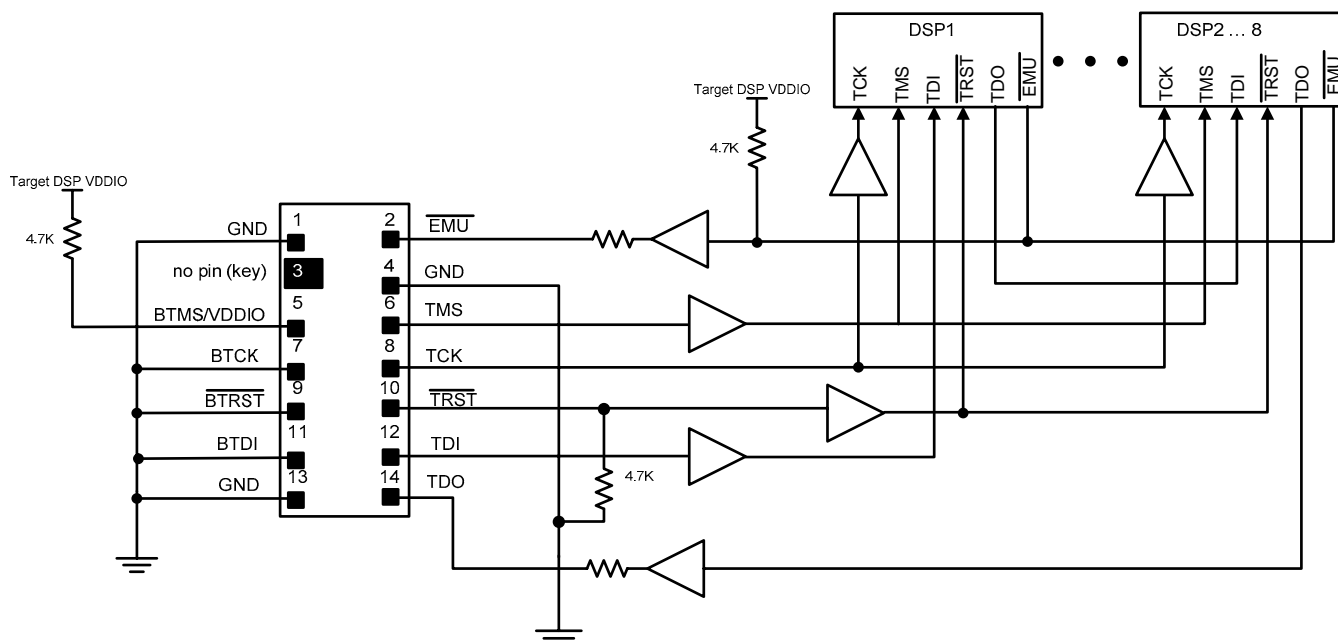

Figure 7. Multiple DSP target without a local boundary scan controller

Appendix C: Target JTAG Interface Design - Single DSP Target with Boundary Scan

This section describes how to design the JTAG emulator pod interface for single DSP targets *with* a local boundary scan controller.

Single DSP targets *with* local boundary scan controller logic should connect the local boundary scan signal pins to the JTAG emulator header pins shown in Figure 8.

If your target has an optional local boundary scan controller, and you attach a HPPCI JTAG emulator, you will need to isolate the BTMS signal from the BTMS/VDDIO voltage pin before starting the emulator software. Referring to Figure 8, during JTAG emulation you can isolate pin 5 on the HPPCI JTAG emulator header from the local boundary scan controller logic using a jumper or three-state buffer.

ⓘ You must provide a method to isolate the BTMS signal on your target from the BTMS/VDDIO pin on the JTAG emulator header when the HPPCI JTAG emulator is connected. Isolation must be effective before the HPPCI JTAG emulator software is invoked. This isolation will prevent the local boundary scan controller BTMS signal from confusing the automatic voltage sensing logic in the HPPCI JTAG emulator pod.

Connections are made between the local boundary scan controller and the DSP by installing or removing jumpers between the local boundary scan controller JTAG signals and the DSP JTAG emulation signals. The local boundary scan signals include BTMS, BTCK, BTDI, and BTRST~. DSP JTAG emulation signals TMS, TCK, TDI, and TRST~ connect to local boundary scan signals using jumpers on the JTAG emulator header shown in Figure 8.

ⓘ TRST~ must be pulsed low at power-up when using a local boundary scan controller, and should be kept low when the local boundary scan controller and the JTAG emulator are not being used. Figure 8 shows how TRST~ should be controlled when the target uses a local boundary scan controller.

If your target has a local boundary scan controller and your target *does not* control the BTRST~ signal, you will need to control the BTRST~ signal with additional logic. This additional logic must guarantee that the BTRST~ signal is only pulsed low during power-on reset. It should be driven high all other times during local boundary scan. This will prevent holding the BTRST~ signal low continuously during local boundary scans.

Keep the DSP TAP constantly in reset with the BTRST~ signal forced to ground with a jumper or pull-down resistor to prevent the DSP from executing a local boundary scan.

ⓘ The 4.7-KΩ pull-down resistor on TRST~ shown in Figure 8 should not be used for targets which have a local boundary scan controller and ***do not*** drive TRST~. The DSP JTAG TAP will be kept constantly in reset when using a pull-down resistor if it cannot be overdriven.

Figure 8 shows the connections between the JTAG emulator header and the DSP for a single DSP target *with* a local boundary scan controller.

ⓘ Jumpers can be substituted with zero ohm resistors on production boards. If you plan to use the same board revision for debugging and production, design your target with a dual footprint. The dual footprint should accommodate the header described in Figure 1 for debug boards, and surface mount resistors for production boards.

Single DSP targets with routing distances between the JTAG emulator header and the DSP of less than six (6) inches do not require buffering.

Buffer your target if the worst-case route distance between the JTAG emulator header and the DSP is greater than six (6) inches, regardless of the number of DSPs in the scan chain path.

Figure 8 shows series terminating resistors for the TDO and EMU~ signals going to the JTAG emulator. These resistors are optional. Use terminators if the TDO or EMU~ routes are longer than 6 inches between the DSP and the JTAG emulator header.

The terminator resistor value is generally equal to the impedance of the printed circuit board (Z_{PCB}) minus the output impedance of the TDO or EMU~ signal I/O driver (Z_{Driver}). Initially, set these resistors to zero ohms. Change the value of the termination resistance $Z_{Terminator,}$ to Z_{PCB} minus Z_{Driver} if signal integrity problems are observed when using the JTAG emulator. Tuning the termination resistor value to something slightly less than or greater than $Z_{Terminator}$ may be required, depending on the condition of the signals. Place the termination resistors as close to the DSP as possible.

Previous versions of this document called for pull-up resistors on TMS, TCK, and TDI. The strong drive strength of the CMOS buffers used in the emulator makes this unnecessary.
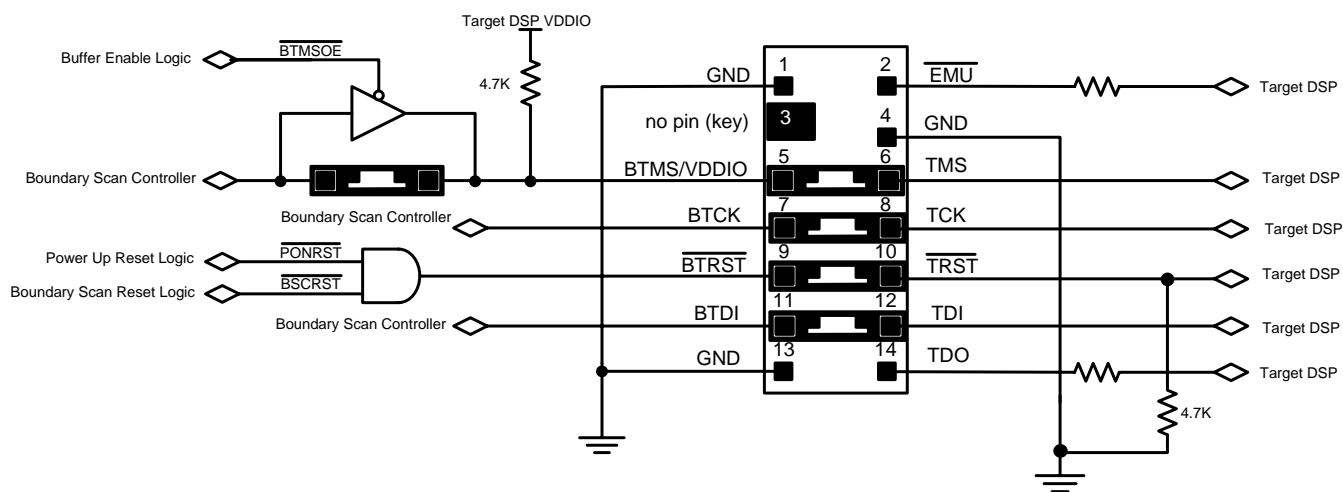

Figure 8. Single DSP target with a local boundary scan controller

Appendix D: Target JTAG Interface Design - Multiple DSP Target with Boundary Scan

This section describes how to design the JTAG emulator pod interface for multiple DSP targets *with* a local boundary scan controller.

Multiple DSP targets *with* local boundary scan controller logic should connect the local boundary scan signal pins to the JTAG emulator header pins shown in Figure 9.

ⓘ Jumpers can be substituted with zero ohm resistors on production boards. If you plan to use the same board revision for debugging and production, design your target with a dual footprint. The dual footprint should accommodate the header described in Figure 1 for debug boards, and surface mount resistors for production boards.

If your target has an optional local boundary scan controller, and you attach a HPPCI JTAG emulator, you will need to isolate the BTMS signal from the BTMS/VDDIO voltage pin before starting the emulator software. Referring to Figure 9 during JTAG emulation, you can isolate pin 5 on the HPPCI JTAG emulator header from the local boundary scan controller logic using a jumper or three-state buffer.

ⓘ You must provide a method to isolate the BTMS signal on your target from the BTMS/VDDIO pin on the JTAG emulator header when the HPPCI JTAG emulator is connected. Isolation must be effective before the HPPCI JTAG emulator software is invoked. This isolation will prevent the local boundary scan controller BTMS signal from confusing the automatic voltage sensing logic in the HPPCI JTAG emulator pod.

Connections are made between the local boundary scan controller and the DSP by installing or removing jumpers between the local boundary scan controller JTAG signals and the

DSP JTAG emulation signals. The local boundary scan signals include BTMS, BTCK, BTDI, and BTRST~. DSP JTAG emulation signals TMS, TCK, TDI, and TRST~ connect to local boundary scan signals using jumpers on the JTAG emulator header shown in Figure 9.

ⓘ TRST~ must be pulsed low at power-up when using a local boundary scan controller, and should be kept low when the local boundary scan controller and the JTAG emulator are not being used. Figure 9 shows how TRST~ should be controlled when the target uses a local boundary scan controller.

If your target has a local boundary scan controller and your target *does not* control the BTRST~ signal, you will need to control the BTRST~ signal with additional logic. This additional logic must guarantee that the BTRST~ signal is only pulsed low during power-on reset. It should be driven high all other times during local boundary scan. This will prevent holding the BTRST~ signal low continuously during local boundary scans.

Keeping the DSP TAP constantly in reset with the BTRST~ signal forced to ground with a jumper or pull-down resistor will prevent the DSP from executing a local boundary scan.

ⓘ The 4.7-KΩ pull-down resistor on TRST~ shown in Figure 9 should not be used for targets that have a local boundary scan controller and *do not* drive TRST~. The DSP JTAG TAP will be kept constantly in reset when using a pull-down resistor if it cannot be overdriven.

As shown in Figure 9, targets with more than one DSP in the scan path, which **do** use a local boundary scan controller, require buffering. Figure 9 shows the connections between the JTAG emulator header and buffers for a multiple DSP target *with* a local boundary scan controller.

For 5-V targets, buffer the `TCK` signal with a low-skew, high fan-out, minimal input-to-output delay, dual 1-to-5 clock driver type IDT49FCT805 (or equivalent), and buffer the `TMS`, `TDI`, `TRST~`, `TDO`, and `EMU~` signals with a type 74AC11244 buffer (or equivalent).

For 3.3-V low-voltage targets, buffer the `TCK` signal with a low-skew, high fan-out, minimal input-to-output delay, dual 1-to-5 clock driver type IDT49FCT3805E (or equivalent), and buffer the `TMS`, `TDI`, `TRST~`, `TDO`, and `EMU~` signals with a type 74AVC16244 buffer (or equivalent).

For 2.5-V / 1.8-V very low voltage targets, buffer the `TCK` signal with a low-skew, high fan-out, minimal input-to-output delay, single 1-to-5 clock driver type IDT5T9050 (or equivalent), and buffer the `TMS`, `TDI`, `TRST~`, `TDO`, and `EMU~` signals with a type 74AVC16244 buffer (or equivalent).

(i) Figure 9 shows series terminating resistors for the `TDO` and `EMU~` signals going to the JTAG emulator. These resistors are optional. Use terminators if the `TDO` or `EMU~` routes between the buffers and the JTAG emulator header are longer than 6 inches.

The terminator resistor value is generally equal to the impedance of the printed circuit board (Z_{PCB}) minus the output impedance of the `TDO` or `EMU~` signal I/O driver (Z_{Driver}). Initially, set these resistors to zero ohms. Change the value of the termination resistance $Z_{Terminator}$ to Z_{PCB} minus Z_{Driver} if signal integrity problems are observed when using the JTAG emulator. Tuning the termination resistor value to something slightly less than or greater than $Z_{Terminator}$ may be required, depending on the condition of the

signals. Place the termination resistors as close to the DSP as possible.

(i) To minimize signal skew, ensure that buffers for the `TMS`, `TDI`, `TRST~`, `TDO`, and `EMU~` signals come from a single package. For `TCK` signals, use a driver with a high fan-out. The drivers should come from a single dedicated package that *is not* used by other `TMS`, `TDI`, `TRST~`, `TDO`, or `EMU~` signals.

Route all traces between the JTAG emulator header and the DSP as a group, using equal lengths when possible. Provide good crosstalk isolation from other signal nets especially clocks.

Limit the number of loads (DSPs) for the `TMS`, `TRST~`, and `EMU~` buffered signals to eight (8). Limit the number of loads for the `TCK` buffered signals to one (1). Additional loads (DSPs) should use another buffer to support up to eight (8) more devices.

(i) Previous versions of this document called for pull-up resistors on `TMS`, `TCK`, and `TDI`. The strong drive strength of the CMOS buffers used in the emulator makes this unnecessary.

Using more than sixteen (16) physical devices in one scan chain is not recommended. The best approach for large numbers (>16) of physical devices is to break the chain into smaller independent chains, each with its own JTAG header and buffers. If this is not possible, try adding jumpers to reduce the number of devices in one chain at a time for debug purposes. Pay special attention to PCB routing to minimize transmission line effects.
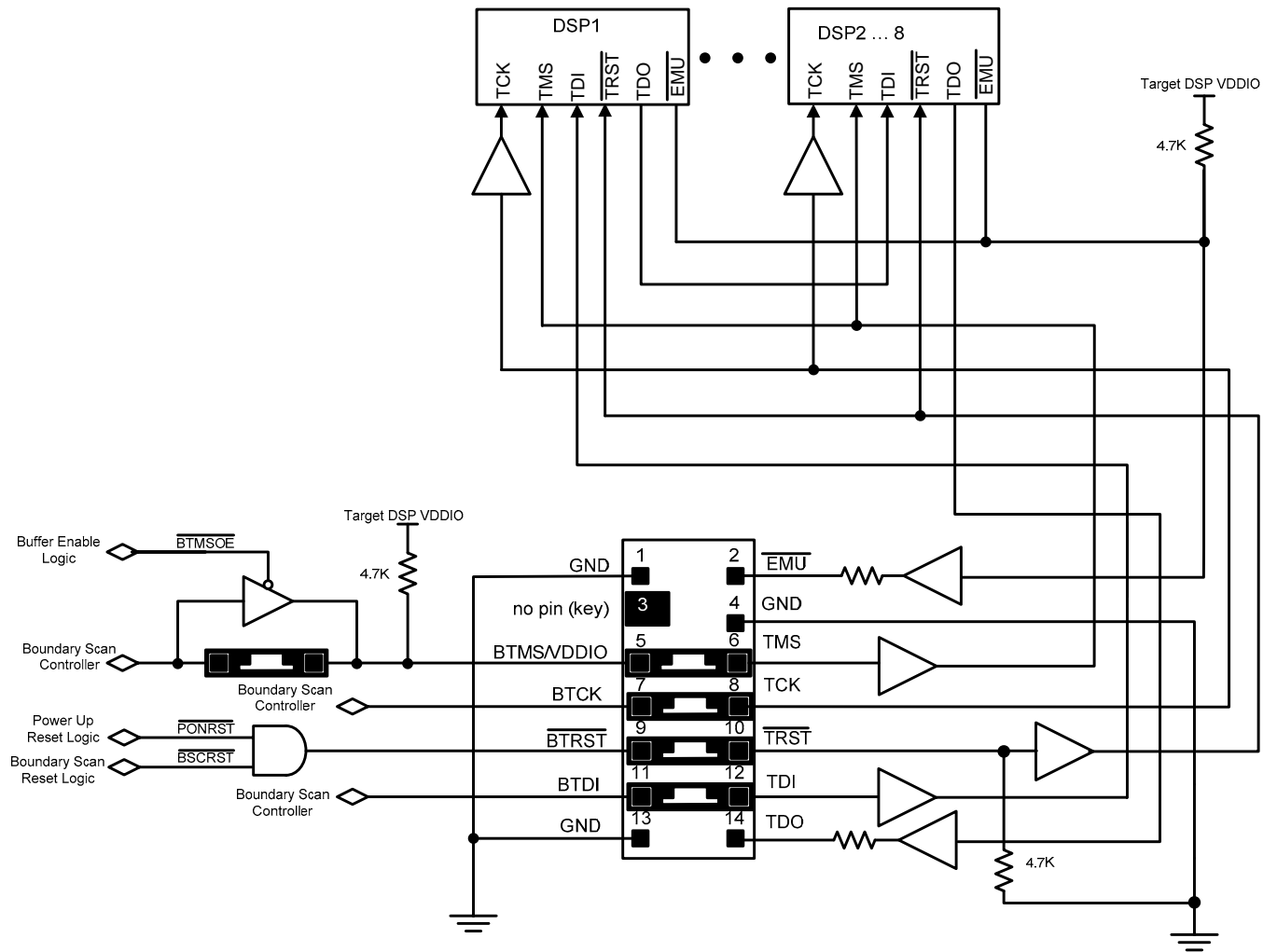
Figure 9. Multiple DSP target with a local boundary scan controller

Appendix E: Introduction to IEEE Std. 1149.1 (JTAG) Boundary Scan

This section is a brief introduction to the IEEE 1149.1 (JTAG) specification and the concept of Boundary Scan for customers who may be unfamiliar with these topics.

IEEE Std. 1149.1 (JTAG) Specification

As printed circuit boards became very dense with complex fine pitched components in PGA and BGA packages, traditional testing methods using bed of nails and in-circuit tests became very difficult if not impossible. A new method needed to be developed to allow testing these complex dense PCBs. To solve this problem, in the 1980s the Joint Test Action Group (JTAG) developed the IEEE Std. 1149.1 standard utilizing Boundary-scan for testing connections on printed circuit boards at the device pin level. The standard was ratified, adopted and first introduced in 1990. Several subsequent revisions to the specification have been adopted including in 1993 revision 1149.1a, and in 1994 a supplement to the specification for a boundary scan descriptive language (BSDL) was introduced. Companies which integrated the IEEE Std. 1149.1 standard into their products (ICs) for board and component testing, have gone further using JTAG for programming FPGAs, downloading micro-code, and in-circuit emulation, etc.

Boundary Scan: What is It?

Boundary scan provides a method for testing interconnects on a PCB without having to use physical probes like a bed of nails. By using internal boundary scan cells with multiplexing and latching capabilities, data can be shifted in and out of device interconnects in a serial format. Each boundary scan cell using its own multiplexer and latch logic is connected to a device pin, and all boundary scan cells are connected forming a serial chain. The chain will include the boundary scan cells for all or some of a device's pins (user defined) which is connected to other devices (user defined) on the PCB.
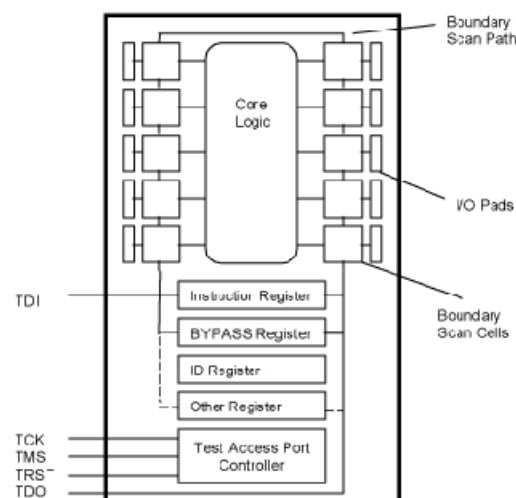

Figure 10. Boundary scan implementation diagram

Figure 10 shows a diagram of how a part implementing IEEE Std. 1149.1 would connect the individual boundary scan cells, and the JTAG controller logic. The pins TDI, TCK, TMS, TDO, and optional TRST~ provide the test access port (TAP) for shifting (TCK) data in (TDI) and data out (TDO) controlled by (TMS). The external device which drives the TCK, TMS, and TDI pins can also reset the TAP controller by driving the optional TRST~ pin. Data is returned to the external device controlling the operation of the TAP with the TDO pin.

Along with boundary scan operations, Analog Devices uses the TAP controller to access dedicated internal registers with JTAG scan cells to shift data in and out of the DSP, providing a port for emulation. Analog Devices does include the optional TRST~ pin in all their current DSP JTAG TAP logic and also uses a dedicated emulation control pin (EMU~) which is not defined as part of the IEEE Std. 1149.1 standard.

If you desire more information on how the IEEE Std. 1149.1 standard works, you can visit their Web site at http://standards.ieee.org/.

References

The IEEE 1149.1 JTAG standard is sponsored by the Test Technology Standards Committee of the IEEE Computer Society, and published by the IEEE.

To order a copy, call IEEE at 1-800-678-4333 in the US and Canada (1-908-981-1393 outside of the US and Canada). You can also visit the IEEE standards web site at http://standards.ieee.org/

Document History

Revision	Description
Rev 10 – April 15th, 2008 by D. Doyle	Major update with the following changes: Corrected Note 10, switching the buffer part numbers for 5V and 3.3V Removed Notation table, and broke up the 4 different Target types (Single or Multi DSP with or without local boundary scan) into Appendixes A through D with individual JTAG Interface design instructions. Updated Figures 5, 6, 7, and 8 showing TRST/ pulled low to ground with a 4.7KΩ resistor. Noted the special case of not using a pull down resistor when an on-board boundary scan controller is being used and TRST/ is not controlled. Updated Figure 2, 3, and 4 showing the physical location of pin 1 on the probe header. Added tables of contents, list of figures, and list of tables at beginning of document to make navigating to target applicable document information sections easier. Removed the requirement for jumpers or zero ohm resistors on the JTAG header for targets that do not implement their own boundary scan controller. Added Appendix E to provide an introduction to the IEEE Std. 1149.1 (JTAG) Standard for customers unfamiliar with the specification.
Rev 9 – October 18th, 2004 by D. Doyle	Major update. Incremented revision code to Rev 9 due to revision system change Removed all obsolete Legacy information. Simplified and combined drawings and tables when possible. Re-wrote most sections in more concise format
Rev 2.6 – July 9th, 2003 by D. Doyle	Updated all document discussions for the TRST~ signal and JTAG Emulation header jumper requirements. Most sections of the document were affected. Changed keep out clearance requirements for larger HPPCI pod.
Rev 2.5 – March 20th, 2003 by D. Doyle	Divided document into discussion of Legacy ICE products and our new HPPCI ICE product. Added HPPCI information
Rev 2.4 – December 3rd, 2002 by D. Doyle	Updated all sections and added timing information

Rev 2.3 – August 2001 *by D. Doyle*	Update to power up sections
Rev 2.2 – March 2001 *by D. Doyle*	Update to target connections
Rev 2.1 – August 2000 *by D. Doyle*	Update for 2.5 logic
Rev 2.0 – February 2000 *by D. Doyle*	General update
Rev 1.0 – December 1999 *by D. Doyle*	Initial release